IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	Confirmation Number: 9226
Su *et al.*	Group Art Unit: 2614
Serial No.: 10/661,492	Examiner: Lao, Lun S.
Filed: September 15, 2003	Docket No.: 251812-1340 RealTek Ref.: 94A-023US

For: **Apparatus for Automatic Identification of Audio Input/Output Device and Method Thereof**

REMARKS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop Appeal
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Despite Applicant's clear distinctions, the FINAL Office Action has maintained all substantive rejections. Applicant files herewith a Notice of Appeal to appeal these rejections. Should an Appeal Brief be necessary, Applicant will resubmit the arguments from its previous response. However, in a desire to expedite the prosecution of this application, Applicant has filed the accompanying pre-appeal brief request for review. Because of the 5-page limit imposed on these remarks, Applicant (below) sets forth on some of the clear errors that are embodied the FINAL Office Action.

Rejections under 35 U.S.C. § 103

The FINAL Office Action rejected claims 24-26, 29-33, and 35 under 35 U.S.C. § 103(a) as being allegedly unpatentable over *Patterson et al.* (US Pub. 2004/0081099, hereinafter *Patterson*). These rejections are clearly erroneous. To begin, independent claim 24 recites:

24. An apparatus for automatically determining a type of an external device, comprising:

a jack for coupling the external device;

an impedance detecting circuit, coupled to the external device through the jack, for generating a first analog signal according to an impedance of the external device and a first resistance, a second analog signal according to the impedance of the external device and a second resistance and a third analog signal according to the impedance of the external device and a third resistance, wherein the first, second and third resistances are different;

an analog-to-digital converter, coupled to the impedance detecting circuit, for converting the first, second and third analog signals to first, second and third digital values, respectively; and

a control circuit, coupled to the analog-to-digital converter, for determining the type of the external device when the first digital value falls within a first predetermined range, the second digital value falls within a second predetermined range, the third digital value falls within a third predetermined range and all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions;

wherein the impedance detecting circuit comprises a plurality of resistors, which couples together in parallel, for providing the first, second and third resistance and each of the first, second and third digital values is a multi-bit number.

(*Emphasis added*). Applicant respectfully submits that *Patterson* fails to disclose, teach, or suggest at least the features emphasized above in claim 24.

One argument advanced in Applicant's previous response was that, regarding the impedance detection circuit, the Office Action (p. 3) alleges that R1, R5, and R6 of FIG. 9B correspond to the first, second, and third resistances, respectively. Applicant notes that the Office Action has not identified features of *Patterson* that allegedly correspond to first, second, and third analog signals that are generated according to the impedance of the external device and the respective resistance. Instead, the Office Action has merely pointed out three different resistors from the reconfiguration circuit 32e.

As more fully explained in Applicant's previous response, that the reconfiguration circuit 32e of Pattersonn has a vastly different function from an "impedance detection circuit" as recited in this feature of claim 24. The reconfiguration circuit "responds to the identification of a particular load at a particular jack by load sensing circuit 30 and reconfigures the circuits associated with that connector so that they are properly adapted for the identified load." ([0045]). Nowhere does *Patterson* disclose, teach, or suggest generating three analog signals in the reconfiguration circuit according to the impedance of the external device concurrently with three different resistances. Furthermore, this Office Action points to resistor R5, which is part of a "programmable microphone bias source controlled by the level on input 260." ([0060]). Thus, even assuming, *arguendo*, that a signal is generated according to R5, the signal is not generated according to the impedance of the external device.

The FINAL Office Action essentially ignored this argument by saying: "The examiner responds that the argued concurrency is not claimed, and thus moot." (FINAL Office Action, p. 12, lines 9-10). While the term "concurrently" may not be expressly used in claim 24, claim 24 does recite that "...***wherein the impedance detecting circuit comprises a plurality of resistors, which couples together in parallel, for providing the first, second and third resistance."*** It is, therefore, expressly clear that the parallel connection between the resistors (to provide the first, second, and third resistances) would ensure that the corresponding analog signals (each of the three analog signals being passed through the respective resistor) would be concurrent. Thus, the Examiner's failure to address this distinction is a clear error.

Another clear error relates to the claim limitation quoted above (i.e., "***wherein the impedance detecting circuit comprises a plurality of resistors, which couples together in parallel, for providing the first, second and third resistance***."). The FINAL Office Action cited resistors R1, R5, and R6 (of FIG. 9B) of Patterson as being

the claimed resistors. As can be readily verified from FIG. 9B of Patterson (relevant portion reproduced below), resistors R1, R5, and R6 are not connected in parallel.

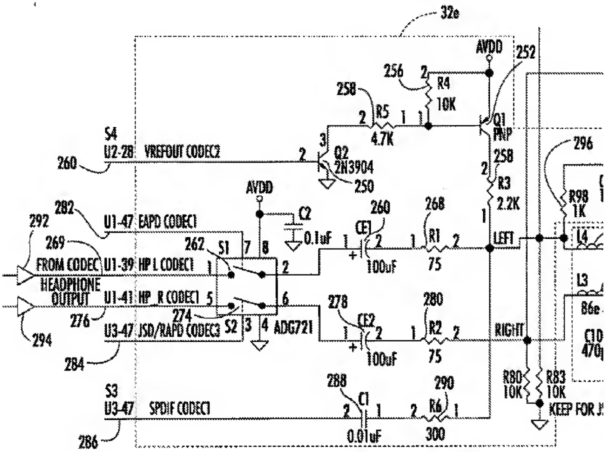

FIG. 9B

Consider, for example, the Examiner's allegation that resistors R1 and R5 are connected in parallel. Resistor R5 is series connected between transistors Q1 and Q2. A drain of Q1 is connected to a terminal or resistor R1 through a resistor R3. The other terminal of resistor R1 is connected to (via relay) either to the "HP L" line of CODEC1 or to the "EAPD" line of CODEC 1 (via series connection through capacitor CE1). In contrast, the opposing terminal (terminal 2) of resistor R5 is connected to the "VREFOUT" line of CODEC2 (via series connection through transistor Q2.

It simply defies logic (and basic electrical engineering definitions of what it means for circuit elements to be connected in "parallel") to suggest that resistors R5 and R1 are connected in parallel (a similar analysis can be made with respect to resistor R6). In this regard, there is NO apparent connection of terminal 2 of R5 with terminal 1 of R1.

This application of Patterson to the express language of claim 24 is clearly erroneous.

There are a number of other erroneous applications of Patterson to the pending independent claims, which were set forth in Applicant's previous response, and which will be detailed in an Appeal Brief, should the filing of a brief become necessary. No further arguments are submitting in this document, in order to remain within the five-page limit. Applicant believes, however, that the foregoing clearly details fundamental errors which warrant the withdrawal of the rejections of the FINAL Office Action.

A credit card authorization is provided to cover the fee associated with the accompanying Notice of Appeal. No additional fee is believed to be due in connection with this submission. If, however, any additional fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,

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